IN THE SPECIFICATION

Please amend the paragraph beginning at page 22, line 14 through page 23, line 6, as follows:

With the extensible processor according to the first embodiment of the present invention, when the instructions for the extension unit 32 [[is]] are also executed with the same clock count as that for the processor core 10, the instructions for the processor core 10 and the extension unit 32 are organized as shown in FIG. 5. The pipeline for the processor core 10 is originally organized from, for example, five stages such as an instruction fetch (F), an instruction decode (D), an execution (E), a memory access (M), and a write-back (W) stage, wherein each stage takes one clock cycle and each stage operates in an overlapping manner. In the case of the instructions for the extension unit 32 being executed with the same clock count as that for the processor core 10, instructions 1, 2, and 3 for the processor core 10 are represented by INS1C, INS2E, and INS3C, respectively, relative to the clock CLK, as shown in FIG. 5.